ABSTRACT

A unified, extra regular, complexity-effective, high-performance multiplier construction method. The method is applicable to a whole spectrum of n x n-b pipelined or non-pipelined multipliers for $10 \leq n \leq 81$, with no more than two levels of tripling process for each construction. The method includes a library containing 3-b to 9-b borrow parallel small multipliers, used for compact, low-power implementation. The multipliers are developed based on the novel counter circuitry, called borrow parallel counter, which utilizes 4-b 1-hot encoded signals and borrow bits, i.e., bits weighted 2. Exampled by a 54 x 54-b (bit) multiplier, the method allows large multipliers to be generated from smaller multipliers, tripling the size in each expansion (6 x 6-b to18 x 18-b to 54 x 54-b). This significantly reduces the complexity of state of the art designs and achieves full self-testability without sacrificing high-performance.